

Printing nanotube-based p-type thin film transistors with high current density

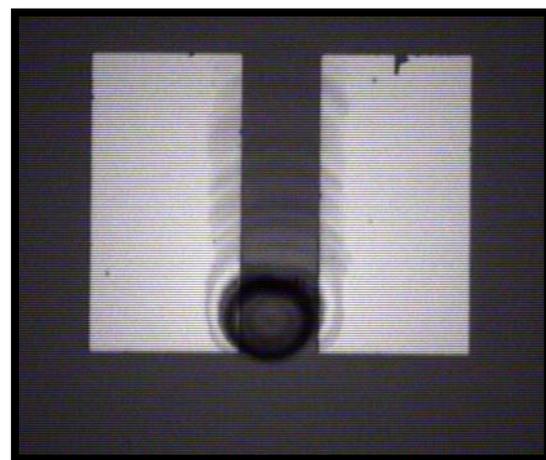
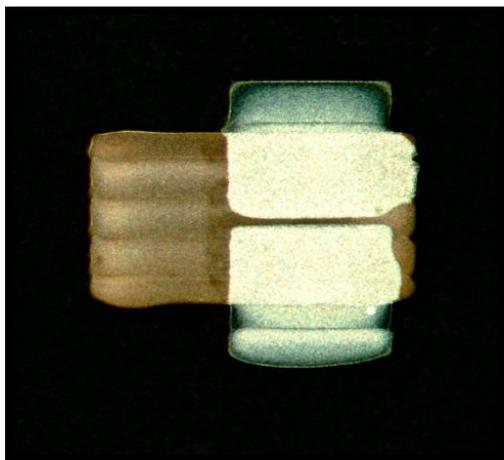
Single-wall carbon nanotubes (SWCNT), with their outstanding mechanical and electrical properties, offer a solution to coat or print high current density (high-mobility) and bendable thin-film transistors for the emerging flexible electronics market. While some materials exist to print high-mobility n-type organic thin-film transistors (OTFT), there are currently only a very few candidates for a p-type high-mobility OTFT material (mobility > 5 cm²/V-s), and semiconducting single wall carbon nanotubes (SC-SWCNT) is one.

The following white paper describes proven methodologies used to coat and print the active material (high purity semiconducting-nanotubes) for thin film transistors. It is based on recent state-of-the-art academic literature and our own experience.

Focus will be on Si/SiO₂ substrates (refs. 1 and 6) for reproducibility of results but flexible substrates such as PET (ref. 2) or Kapton™ polyimide (ref. 3) and even transparent substrates such as glass (ref 4.) may be preferable. For example, a silicon wafer designed to test organic semiconductor materials is an easy test system that should allow to obtain good performances before moving on to more challenging substrates.

As semiconducting nanotube solutions can be obtained either in aqueous or organic solvents, differences in processing will be discussed. The main steps involved in the process, common to all solvents and substrates, are (A) verification of nanotube dispersion and concentration, (B) substrate surface preparation to ensure SWCNT adhesion, (C) film deposition with adequate nanotube density, and (D) rinsing and annealing. Nanotube film encapsulation is not discussed but is beneficial to diminish hysteresis in transfer characteristics (ref. 5). Dielectric layer, gate and contact deposition will not be discussed explicitly as different circuits require different transistor architectures, but further reading on the topic is suggested (see references 1-6 as well as references therein). For those less familiar with these aspects, we recommend starting with a commercially available silicon wafer with pre-fabricated source/drain electrodes on SiO₂ (see ref. 7 for one potential supplier). If done correctly, this procedure leads to p-type transistors (when tested in ambient air) with performances that reliably match those published in the scientific literature. Nanotube-based thin-film transistors (SWCNT-TFT) deliver average mobilities of 10-20 cm²/V-s and current ON/OFF ratios of 10³-10⁶ on Si substrates using SiO₂ as the gate dielectric as well as average current densities of 1-10 μA/μm, sufficient in principle to drive organic light-emitting diodes (OLEDs). Typical performance targets for OLED applications are 10⁶ in ON/OFF ratio and mobilities greater

than $10 \text{ cm}^2/\text{V}\cdot\text{s}$, coupled to less than 0.1 Volts in threshold voltage variability. With proper encapsulation, SC-SWCNT are strong candidates to drive OLEDs. For those interested in measuring the transfer characteristics and evaluating the performance of nanotube transistors printed on Si/SiO₂, they can be purchased directly from NanoIntegris (see contact information at the end of the text).



Left: Fully Inkjet Printed Thin-Film Transistor on PET. Right: Fully inkjet printed SWCNT channel with evaporated Ti/Pd contacts on a high k dielectric. Both images were produced by the CNRC-NRC.

A. Verification of nanotube dispersion and concentration

The semiconducting carbon nanotube concentration of an ink (in weight of nanotubes per volume of ink) has a big impact on the number of printing passes necessary to achieve the nanotube density required (see section C), but will also impact ink stability and shelf life. Typically, NanoIntegris water based inks (IsoNanotubes-S) have a concentration of 0.01 mg/ml and the organic solvent-based inks have a concentration of 0.05 mg/ml. This latter concentration can be raised upon request up to 1 mg/ml.

As nanotubes have a large surface area and thus attract strongly due to Van der Waals interactions, nanotubes dispersed in solutions will tend to bundle and aggregate on time scales that depend on nanotube density and surfactants used for the dispersions. Nanotubes in aqueous solution have a shelf life of 3 months starting after the day of production and should be used within that period for optimal performance, as bundling and aggregation will lead to lower performances. If aggregates can be seen upon visual inspection, please contact us for advice.

Organic solvents such as methanol or acetone should **not be mixed** with aqueous nanotube solutions as they will remove surfactants from the semiconducting nanotubes and lead to strong bundling and aggregation.

Nanotubes in organic solvents are wrapped by conjugated polymers and are thus less prone to bundling and aggregation (ref 1.). The shelf life of NanoIntegris semiconducting nanotubes in organic solvents is thus 6 months rather than the 3 months for aqueous solutions. Furthermore, **a gentle bath sonication will restore the initial nanotube dispersion** and should be carried out prior to use for optimal performance.

B. substrate surface preparation to ensure CNT adhesion

Si/SiO₂ Substrate

This step is **critical for water-based** SWCNT inks (such as IsoNanotube-S) on SiO₂ or PET but is **not or less necessary with organic-solvent** based SWCNT inks as the polymers wrapping the tubes allow much better adhesion. Especially for SiO₂ substrates, the wafer cleaning is essential and can be done with Piranha solution (see Annex 1 for a detailed method to clean silicon wafers).

1. If you take a silicon wafer (chip) with a 100 nm thick thermal oxide layer, clean using Piranha solution (1 : 2 (v/v) of 98% H₂SO₄ and 35% H₂O₂) for 30 min at 80 °C. After thoroughly rinsing with distilled water and isopropanol, blow the chip dry with nitrogen.
2. If you are using the NanoIntegris organic solvent-based ink, you are ready to print! If you are using a water-based ink, it is necessary to deposit an adhesive coating such as Poly-L-Lysine (PLL) or APTES (3-Aminopropyl)triethoxysilane).
3. If you choose Poly-L-Lysine as the adhesive (refs. 1,3), mix 0.5-1 mL of Poly-L-Lysine (PLL) with 20 ml of DI water and pour into a vial. Add the chip and make sure there is sufficient solution covering the test chip. Leave undisturbed for 5 minutes. Pour PLL solution into waste, add 20 mL of DI water to the vial, swirl, and pour solution into waste. Repeat 10 times or until you have used ~200 mL of DI water.
4. If you choose APTES (ref. 6) as the adhesive, dilute 0.1 g of ATPES in 200 ml of DI water and mix. Soak wafer overnight, then rinse with DI water to remove excess APTES by squirting DI water over wafer for 10 seconds. Let dry in air or blow dry with nitrogen. You are now ready to print the nanotube active layer.

For a Polyethylene (PET) or Polyimide Substrate

For flexible substrates and bottom gate configuration, the surface preparation depends largely on the choice of dielectric layer that covers the gate located immediately over the substrate. We direct the reader to references 2 and 3 for different dielectrics and surface preparations. Reference 2 describes how a flexible PET substrate is coated with Poly-L-Lysine to maximize nanotube adhesion.

Reference 3 describes how 20 nanometers of Al₂O₃ and 15 nm of SiO_x are deposited over polyimide using atomic layer deposition and e-beam evaporation, respectively, to serve as the gate dielectric. Following this step, the deposition of an adhesive layer such as PLL is required to ensure that the nanotubes stick to the thin silicon oxide layer.

C. film deposition with adequate tube density

The SWCNT ink can be printed **using inkjet** printing such as the Fujifilm **Dimatix** Materials Printer (DMP-2800) or the **Ceradrop** system, for example. Using an ink droplet volume of 10 pL, the droplet size should be close to 25µm in diameter. Repeat printing until optimal and even SWCNT film is deposited across entire channel (see below for criteria). The **Sonoplot** printing system has also been used with a 30 µm tip (see reference 3). The **Optomec** aerosol jet printer is another system that has been used with SWCNT inks.

The SWCNT ink can **also be drop-casted** using a pipette. Pipette exactly 40 μL of a SWNT dispersion onto the substrate. Use the tip of the pipette to ensure the solution is spread over the channel area. After deposition, lightly tilt the wafer to drain excess solution.

Optimal tube density is critical as a high tube density (**over $>50/\mu\text{m}^2$**) increases mobility and current density but decreases ON/OFF ratio. Indeed, a higher tube density increases the number of metallic SWCNT present in the film and thus current leakage. In our opinion, optimal tube density lies between **20- $50/\mu\text{m}^2$** and will lead to an optimal trade-off between mobility and ON/OFF ratio. This will also depend on the channel length in which case denser films will be better tolerated at longer channel lengths. After the film is deposited, allow to sit undisturbed for 10-15 minutes.

D. Rinsing and annealing

In all cases, TFT chips should be rinsed with the same solvent as the one initially used to disperse the nanotubes (DI water followed by isopropanol for aqueous solutions and toluene for organic solutions). The use of a squirt bottle and 10 seconds of squirt time are adequate for laboratory settings. The rinsing step will reduce the amount of surfactant or polymer, improve the nanotube-nanotube contact and thus improve performances. While the rinsing step is critical for the water-based inks, the organic-based inks can provide decent performances without this step as the polymer to nanotube ratio in the organic solvent ink is lower than the surfactant to nanotube ratio in the water-based ink. However, the rinsing step improves the performances for all ink formulations and is thus recommended. After rinsing, dry the film with a nitrogen or filtered air stream.

An annealing, or curing, of the nanotube network at 120-200 $^{\circ}\text{C}$ for 15-60 minutes (if the substrate and dielectric can withhold these temperatures) will stabilize the film. This step will decrease the nanotube-electrode contact resistance and the nanotube-nanotube contact resistance and thus increase network conductivity. If the substrate and other layers cannot withstand these temperatures, a lower temperature annealing is recommended as it will increase performances. Steps (c) and (d) should be repeated if microscopy inspection or further analysis reveal that the nanotube density in the film is lower than necessary to attain percolation.

Contact and gate deposition

Please read through references 1-6 for instructions to deposit gates and source and drain contacts on the different substrates and with different materials. For example, titanium and palladium top contacts and bottom gate configuration on SiO_2 is achieved through a shadow mask using an e-beam evaporator. Follow methods described in reference 1. A similar bottom gate (silicon wafer) and top contact configuration is illustrated in reference 5. While the doped p-type silicon wafer acts as the gate, the titanium/palladium source-drain contacts are deposited using shadow mask and electron beam evaporation. Reference 2 describes a top contact (silver source and drain) and top-gate configuration on PET using reverse-gravure printing. A high- κ barium titanate dielectric layer is deposited between the gate and the nanotube layer. Reference 3 illustrates a top-contact and bottom gate configuration on polyimide. After the titanium-gold gate is defined using photolithography and lift-off, top-contacts (titanium and palladium) are created using photolithography. Aluminum and silicon oxide dielectric layers are deposited using atomic layer deposition and electron beam evaporation. After the nanotube channel layer, the titanium/palladium source and drain electrodes are deposited using photolithography. Reference 4

describes a bottom contact (metallic nanotube source and drain) and top gate (ionic gel) configuration achieved using inkjet printing.

References

1. Enrichment of large-diameter semiconducting SWCNTs by polyfluorene extraction for high network density thin film transistors. J. Ding et al. *Nanoscale* 6, 2328-2339 (2014).
2. Fully Printed, High Performance Carbon Nanotube Thin-Film Transistors on Flexible Substrates. P. Heng Lau et al., *Nano Letters* 13, 3864–3869 (2013).
3. Extremely Bendable, High-Performance Integrated Circuits Using Semiconducting Carbon Nanotube Networks for Digital, Analog, and Radio-Frequency Applications. C. Wang et al., *Nano Letters* 12, 1527–1533 (2012).
4. All-printed and transparent single walled carbon nanotube thin film transistor devices. F. Sajed and C. Rutherglen. *Applied Physics Letters* 103, 143303 (2013).
5. Highly stable hysteresis-free carbon nanotube thinfilm transistors by fluorocarbon polymer encapsulation. Tae-Jun Ha et al. *ACS Applied Materials & Interfaces*, DOI: 10.1021/am5013326 (2014).
6. Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications. Chuan Wang et al. *Nano Letters* 9, 4285 (2009).
7. http://www.ipms.fraunhofer.de/content/dam/ipms/common/documents/end-of-line-substrates_stand_E-Mail.pdf

Table 1: Rheological Properties of aqueous semiconducting carbon nanotube solutions sold by Nanolntegris

Semiconducting Ink Properties	
Viscosity (Pa·s)	0.0021
Reynolds number	86-143
Weber number	18-49
Z number	20

Table 2: TFT performances on SiO₂ reported in reference 1.

Dielectric	SiO ₂
Mobility (cm ² /V/s)	20-40
I _{on} /I _{off} ratio	1 x 10 ⁵
Channel Length x Width (μm)	25 x 100
On Current (μA)	>50

Annex 1: Detailed substrate preparation for optimal adhesion on SiO₂

1. Place one Fraunhofer test chip into a 5 dram scintillation vial.
2. Add ~15 mL of acetone to the vial, swirl, and pour acetone into waste but leave the chip in the vial. Note: *the acetone will no longer be colourless*. Repeat 5 more times or until you have used ~100 mL of acetone.
3. Add ~ 1.5 mL of Hellmanex and ~15 mL of MilliQ water to the vial.
4. Heat the vial on a hot plate at 70°C for 30 minutes.
5. Pour cleaning solution into waste, add 20 mL of MilliQ water to the vial, swirl, and pour solution into waste. Repeat 20 times or until you have used ~400 mL of MilliQ water.
6. Add 0.5-1 mL of Poly-L-Lysine (PLL) to the vial; ensure there is sufficient solution covering the test chip. Leave undisturbed for 5 minutes.
7. Pour PLL solution into waste, add 20 mL of MilliQ water to the vial, swirl, and pour solution into waste. Repeat 10 times or until you have used ~200 mL of MilliQ water.

For more details, visit www.nanoIntegris.com or www.nrc-cnrc.gc.ca/eng/news/releases/2013/pe_backgr.html

